HMC Controller IP

OVERVIEW

The Hybrid Memory Cube (HMC) is a high-performance memory solution that delivers unprecedented levels of bandwidth, power efficiency, and reliability. Pico Computing's innovative HMC controller IP unlocks the HMC's power, providing tremendous benefits to memory-bound applications, and particularly to those that require high bandwidth and fast random access. Fully-compliant HMC Rev 1.1 specification, the HMC controller IP is Micron-tested and validated, with support for Altera Stratix V, Xilinx UltraScale®, and Xilinx Virtex-7 series FPGAs.

APPLICATIONS

Pico Computing's high-performance systems solutions dramatically accelerate algorithms with 100 to >1,000X speedups. But when those applications require large amounts of random access memory, performance hits a wall. The HMC solution changes that equation, effectively knocking down the memory wall. When managed by Pico Computing's powerful HMC Controller IP, the new memory technology enables a huge leap forward for high-performance computing, and in the process, opens up new applications, markets, and business models. With a 15x speedup over DDR memory, massive performance improvements are realized immediately in packet processing, waveform processing, bioinformatics, image and video processing, and other memory/bandwidth-bound applications.

FEATURES

Low-level PHY

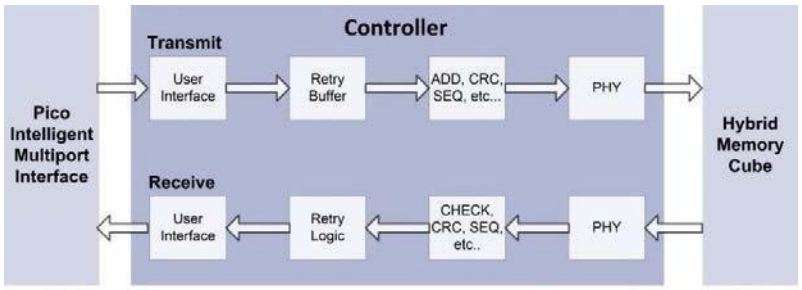
- 8- (half-width) or 16-lane (full-width) full duplex serialized links
- 10Gbp/s (250MHz core); 12.5Gbp/s (312 MHz core); 15Gbp/s (375 MHz core) SerDes I/O interfaces
- Link retraining
- Scrambling and descrambling
- Lane bonding

High-level Controller

- Packet-based data/command interface
- Multiple interface options for maximum flexibility:
  - Full custom interface
  - AXI-4-like interface
  - 640 bit-wide "native" interface
  - Pico Computing's high-performance (intelligent multiport) interface
- Up to 240 GB/s of total interface bandwidth
- Parameterized number of user interface ports
- Flexible datapath widths
- Link layer and transaction layer
- Read/write packet sizes of 16- to 128-byte requests (in 16-byte increments)
- 32-bit address/data bus interface for control and status
- I^2C bus master for HMC bring-up and control
- Atomic commands and bit-write operations supported
- Power-on initialization
- Power state management (per link)
- Poisoned packets, CRC/packet integrity, tagging
- Bit error injection mechanisms to support testability and characterization
- Error detection and automatic retry
- JTAG
- Configuration and status registers
- Warm reset
- TX and RX Link Retry
- Token-based flow control for FPGA-to-HMC direction; open loop response mode for HMC-to-FPGA direction

IP Block Diagram

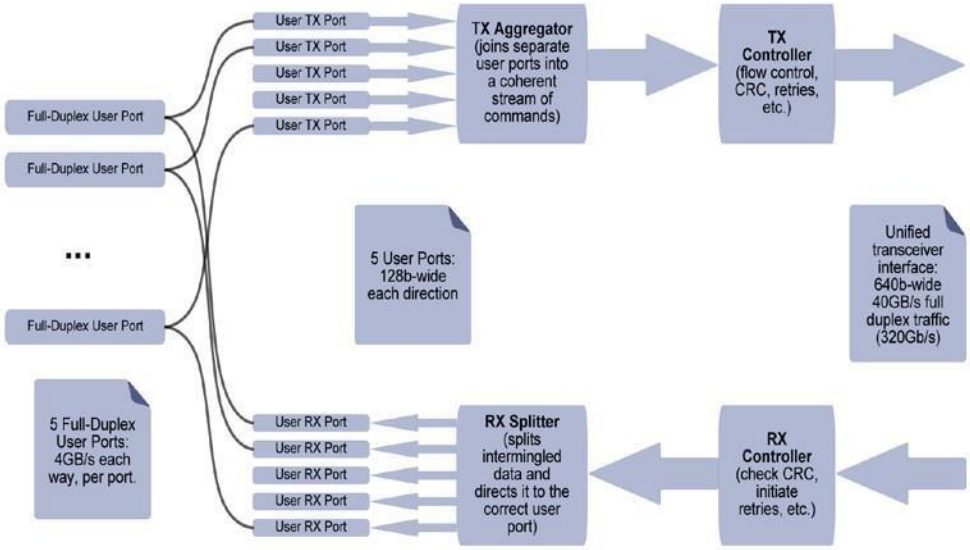
Integration of Pico Computing's HMC Controller is made easy and seamless via multiple interface options (shown at right) that provide data throughput sufficient to satisfy the high memory bandwidths possible with HMC technology.



InterfaceOptions

The HMC IP is available with four user interface options:

1. Full custom interface.
2. 640bit-wide"native"interface.
3. AXI-4-like interface.
4. Pico Computing's high-performance (intelligent multiport) interface. As shown at right, this option breaks the 640 bit-wide native interface into a more manageable set of five 128 bit-wide interfaces. Features round-robin arbitration and response data routing to/from the five user ports. It is low overhead, generates transmit and receive pipelines, handles all send/receive data requests, and makes using the HMC seamless and without adding latency.



HMC block diagram shown with Pico Computing's High-performance Interface option.

Fully Configurable IP

Pico Computing's HMC controller is highly parameterized to yield truly optimized system configurations to meet specific design objectives. The number of HMC links addressed, the number and width of internal ports, clock rate, power, performance, area, and other parameters can be "dialed in" to yield precisely the characteristics required.

Deliverables & Support

Pico Computing offers a complete solution for the HMC Controller, including:

- The complete HMC Controller 1.1 specification in IP, ready for implementation
- Software support
  - HMC link bring-up
  - Direct host software accesses to the HMC with ReadRam(), WriteRam() functions
- RTL
- Bus functional model (BFM) for RTL simulation
- Test bench with simulation model
- Built-in analysis features that allow the evaluation, test, and characterization of the HMC in the context of the system
- The Pico Computing Framework
  - PCIe, DMA engine, APIs, etc.
- User Guide
- Design examples
- Training and application support

Pico Computing's HMC Platforms

AC-510 Xilinx UltraScale FPGA with Hybrid Memory Cube:

- Kintex UltraScale 060 FPGA
- Hybrid Memory Cube:
  - 2GB or 4GB
  - 2x half-width (x8) links
  - 15Gb/s transceivers
- Bandwidth: up to 60 GB/s
- Each half-width (x8) link provides up to 30 GB/s for both RX and TX
- PCIe: x8 Gen 3 PCIe Upstream
- OpenCL support
- Easy design framework with simple FPGA bitstream loading from Host

AC-520 Altera Arria 10 FPGA with Hybrid Memory Cube:

- Altera Arria 10 GX1150 FPGA
- Hybrid Memory Cube:
  - 2GB or 4GB
  - Four half-width (x8) links with 15Gb/s transceivers
- HMC bandwidth: up to 120 GB/s
- 16GB DDR4 SODIMM
- PCIe: Gen 3 x8
- OpenCL support
- Easy design framework with simple FPGA bitstream loading from Host

SB-801 Single-board HPC Solution (Blade Server/Evaluation & Development Board) with Altera FPGA and Hybrid Memory Cube:

- Full height, full length, PCI Express Gen 3 board.
- Array of four Altera Stratix A7 FPGAs sharing a four-link 4G HMC.
- 16GB of DDR3L SDRAM.
- One 10Gb full-width 16-lane link per FPGA to the HMC

Powerful Design Framework

Implementation of the HMC controller is made easy by virtue of Pico Computing's framework, a Linux-based design utility/runtime environment that provides the vital link between your application software running on a host computer and the hardware algorithm, or firmware, implemented in the FPGA. Think of it as the "Ghost in the Machine"—a powerful but invisible and active intelligence that runs and governs the board-level implementation of FPGA designs, as well as data flow, memory management, system communication, monitoring/debug, and more in ways that make life easy for the FPGA design engineer using vendor tool flows. In short, it's everything you need to get up and running right away.

- Automatically loads the HMC controller and other FPGA bitfiles over PCIe
- Includes all drivers including host-side (Unix), interface to host (PCI Express)
- PicoAPI(C++)
- Integrated firmware test suite
- Automates all reading and writing to the FPGAs' off-chip memory (firmware memory interfaces automate all memory systems arbitration)
- Actively monitors FPGA(s) temperature, current, and voltage to enhance system performance and reliability